AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently amended) A heterostructure semiconductor device comprising:

a substrate;

a buffer layer on the substrate;

an active layer on the buffer layer, the active layer comprising at least one group III element and N; [~~and~~]

a composite layer on the active layer, the composite layer comprising:

a strain matching layer over the active layer, the strain matching layer comprising three group III elements and N; and

a barrier layer on the strain matching layer, the barrier layer comprising at least one group III element and N; and

at least one contact over the active layer and adjacent to the composite layer.

2. (Original) The device of claim 1, further comprising a gate on the barrier layer.

3. (Currently amended) The device of claim 1, ~~further comprising:~~ wherein the at least one contact comprises:

a source contact on the active layer; and

a drain contact on the active layer.

4. (Original) The device of claim 3, wherein the strain matching layer and the barrier layer contact both the source contact and the drain contact.

5. (Original) The device of claim 1, further comprising:

a dielectric layer on the barrier layer, wherein the dielectric layer includes Si; and

a gate on the dielectric layer.

6. (Original) The device of claim 1, wherein the substrate comprises one of the group consisting of: sapphire, SiC, spinel, Si, bulk GaN, bulk AlN, or bulk AlGaN.

7. (Original) The device of claim 1, wherein the device comprises one of the group consisting of: a photodetector, a field effect transistor, a gated bipolar junction transistor, a gated hot electron transistor, a gated heterostructure bipolar junction transistor, a gas sensor, a liquid sensor, a pressure sensor, a multi-function sensor, a power switching transistor, and a microwave transistor.

8. (Currently amended) A field effect transistor comprising:

a substrate;

a buffer layer on the substrate, the buffer layer comprising AlN;

an active layer on the buffer layer, the active layer comprising GaN; [~~and~~]

a composite layer over the active layer, the composite layer comprising:

a strain matching layer over the active layer, the strain matching layer comprising AlInGaN; and

a barrier layer on the strain matching layer, the barrier layer comprising AlGaN; and

at least one contact over the active layer and adjacent to the composite layer.

9. (Original) The transistor of claim 8, wherein the composite layer further comprises a quantum well layer directly below and in contact with the strain matching layer, wherein the quantum well layer comprises InGaN.

10. (Original) The transistor of claim 9, further comprising a second strain matching layer on the active layer and directly below and in contact with the quantum well layer, wherein the second strain matching layer comprises AlInGaN.

11. (Currently amended) The transistor of claim 10, further comprising:

a gate on the barrier layer; and

wherein the at least one contact comprises:

a source contact on the second strain matching layer; and

a drain contact on the second strain matching layer.

12. (Currently amended) The transistor of claim 9, ~~further comprising:~~ wherein the at least one contact comprises:

a source contact on the active layer; and

a drain contact on the active layer, wherein the quantum well layer contacts both the source contact and the drain contact.

13. (Original) The transistor of claim 12, wherein the portions of the strain matching layer and the gate barrier layer directly below a gate do not contact at least one of the source contact and the drain contact.

14. (Original) The transistor of claim 8, further comprising:

a dielectric layer on the barrier layer; and

a gate on the dielectric layer.

15. (Original) The transistor of claim 14, wherein the dielectric layer comprises at least one of the group consisting of: SiO_2 and SiN.

16. (Currently amended) The transistor of claim 8, ~~further comprising:~~ wherein the at least one contact comprises:

a source contact on the active layer;

a drain contact on the active layer; and further comprising

a gate on the barrier layer, wherein a distance from the gate to the drain contact is greater than a distance from the gate to the source contact.

17. (Original) The transistor of claim 16, wherein the portions of the strain matching layer and the gate barrier layer directly below the gate do not contact at least one of the source contact and the drain contact.

18. (Original) A field effect transistor comprising:

a substrate;

a buffer layer on the substrate, the buffer layer comprising AlN;

an active layer on the buffer layer, the active layer comprising GaN; and

a composite layer, the composite layer comprising:

a quantum well layer over the active layer, wherein the quantum well layer comprises InGaN;

a strain matching layer on the quantum well layer, the strain matching layer comprising AlInGaN; and

a barrier layer on the strain matching layer, the barrier layer comprising AlGaN.

19. (Original) The transistor of claim 18, further comprising a second strain matching layer on the active layer and directly below and in contact with the quantum well layer, wherein the second strain matching layer comprises AlInGaN.

20. (Original) The transistor of claim 18, further comprising a dielectric layer on the barrier layer, wherein the dielectric layer comprises at least one of the group consisting of: SiO_2 and SiN.